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MONOLITHIC 40 to 60 GHz LNA

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ABSTRACT

Broadband monolithic GaAs MESFET LNAs have been developed to operate over the entire U-band (40 to 60 GHz). These U-band amplifiers make use of state of the art sub .2um MESFET devices. Typical performance for a two stage LNA using 75um devices is at least 7dB of gain with about 1.5dB peak-to-peak ripple and a maximum noise figure of 7.5dB across the 40 to 60GHz band.

INTRODUCTION

Recent advances in GaAs low noise MESFET technology have made it possible to build broadband LNAs at U-band. Although the results published to date show gain through Ka-band [1,2], no broadband monolithic data covering the U-band has been published. This paper describes some of the first monolithic LNAs with reactive matching that cover the full U-band. These chips make use of a sub .2 um MESFET process to achieve less than 7.5 dB of noise figure with more than 7 dB gain for a two stage amplifier. Although the noise figure of these MESFETs is slightly higher than that of a HEMT, they are still good candidates for monolithic integration since the yields are high and the performance is predictable. Monolithic amplifiers recently reported in the literature [2] using HEMT devices do not show significantly superior performance to these MESFET chips.

DEVICE AND FABRICATION

The devices used in this monolithic design were made using either VPE or MBE materials. Both materials produce similar device performance and the VPE material is preferred for production runs since it is a less expensive material.

The gates were defined using electron-beam lithography resulting in gate lengths ranging from .12 to .17um. The gate cross sectional area was also increased by making it in the shape of a mushroom in order to reduce gate parasitic resistance. Figure 1 shows a SEM micrograph of the typical cross section of the mushroom gates.

The device used in this design is a 75 um device with a T layout which consists of a single feed perpendicular to two gate fingers of 37.5 um length.

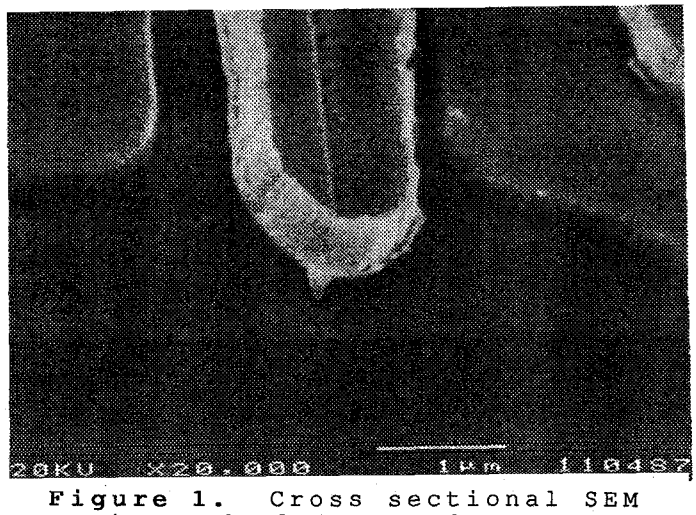


Figure 1. Cross sectional SEM micrograph of the sub .2um mushroom gate.

From measured S-parameters, the F_t is higher than 60 GHz and the F_{max} is higher than 120 GHz for these MESFETs. Figure 2 shows the maximum stable gain and the current gain for the 75um device measured with an on-wafer probe S-parameter system up to 26.5 GHz. From this data one can observe that the K-factor is less than 1 at 26.5 GHz. This is due to the reduced parasitics in the device design thus conserving all the available gain and power produced by the active area of the device.

The typical dc characteristics of these devices are an I_{dss} of 25 mA (.33A/mm) with a pinch-off voltage of -1 V and a transconductance of 30 mS (.4S/mm). The I_{max} for the devices is typically 45 mA (.6A/mm) which occurs at a gate bias of +0.8 V and a dc gate to drain breakdown of 10 V.

Typical performance of these devices when tuned narrowband in a hybrid circuit at 60 GHz is 5dB gain with 4dB noise figure. Other MESFET structures with lower noise figures are available (3dB at 60 GHz) but these monolithic runs made use of an inferior low noise device since they were also optimized for power. Although these devices have slightly higher noise figures than the HEMT counterparts, they remain as excellent production parts and are good candidates for monolithic implementation since the yields are high and the performance is predictable.

The monolithic design made use of via-holes for source grounding, air-bridges for interconnect, and MIM capacitors using silicon nitride for RF grounding and dc blocking. In order to increase the yield and avoid reliability problems, the MIM capacitors were not placed on top of via holes in this design.

TWO STAGE MONOLITHIC AMPLIFIER

A two stage monolithic design has been implemented so that more gain per monolithic chip is obtained. The overall size of this chip will also be smaller than cascading two single stage chips since matching to 50 ohms between stages is not necessary. This achieves more gain per unit area of GaAs used.

The U-band monolithic design relied on accurate device modeling in order to have a first cut success. The model was derived from s-parameter data

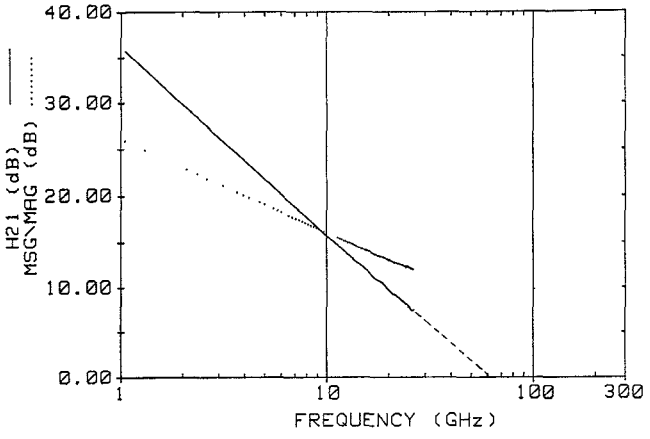
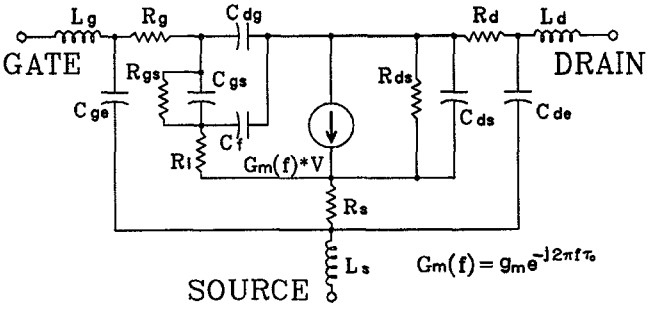


Figure 2. H_{21} and MSG from measured S-parameters for a 75x.2 um low noise MESFET, indicating an F_t of 60 GHz and an F_{max} of 120 GHz.



MESFET	75 μm
g_m (mS)	30
τ_o (ps)	0.5
R_{gs} (Ω)	20000
R_i (Ω)	1.2
R_{ds} (Ω)	475
C_{gs} (pF)	.076
C_{dg} (pF)	.01
C_f (pF)	.018
C_{ds} (pF)	.005
R_g (Ω)	0.8
R_d (Ω)	1.5
R_s (Ω)	2.2
L_g (nH)	.01
L_d (nH)	.01
L_s (nH)	.025
C_{ge} (pF)	.01
C_{de} (pF)	.002

Figure 3. Small signal model for a 75x.15 um low noise MESFET.

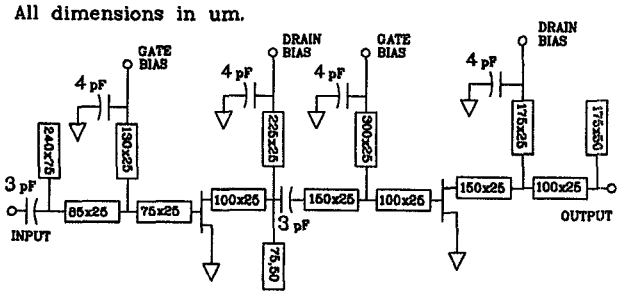


Figure 4. Equivalent circuit and element values for the 40 to 60 GHz monolithic amplifier.

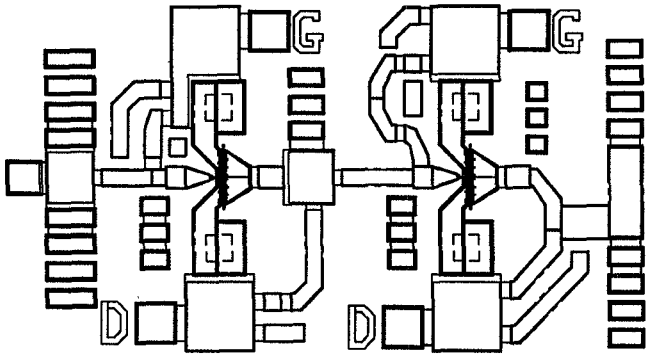


Figure 5. CAD layout for the monolithic amplifier operating from 40 to 60 GHz.

taken up to 26.5 GHz. With the aid of on wafer probing, accurate s-parameter data was available which made it easy to construct an accurate small signal model. The element values of the 75um device used in this monolithic design are shown in Figure 3.

Small signal analysis was then used to establish a broadband design. The equivalent circuit and element values for this two stage design is shown in Figure 4. Both input and output matching circuits consisted of a similar two pole matching topology. The topology consists of a series transmission line from the FET followed by an inductive transmission line to ground via an MIM capacitor which is also used for biasing. These two elements are then followed by another series transmission line and shunt capacitive stub. The interstage matching also consisted of a two pole matching topology. Starting at the output of the first stage, the topology consists of a series transmission line followed by an inductive transmission line to ground via an MIM capacitor which is used for biasing the drain of the first stage. At this point, a dc blocking capacitor (2 pF in value) is added in series. Due to the high value of capacitance, at 40 GHz this capacitor does not contribute much to the RF circuit other than the stray capacitance to ground introduced due to its physical geometry. The circuit is then followed by another series transmission line, an inductive transmission line to ground (also used to bias the gate of the second stage), and another series transmission line. Use of these two pole matching networks made it feasible to obtain a flat response across the desired U-band.

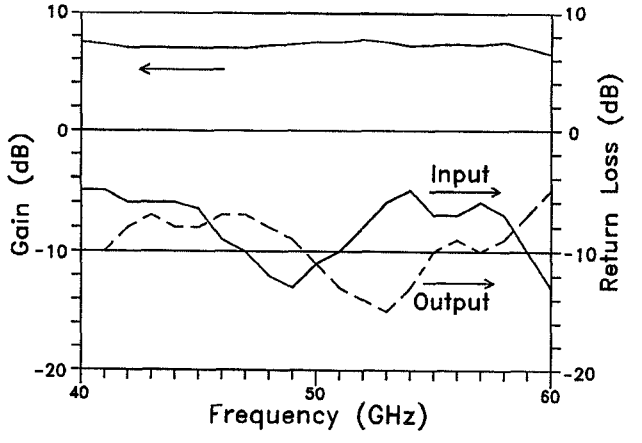


Figure 6. Measured gain and return loss performance for the monolithic two stage amplifier using 75 um MESFET devices.

A CAD layout implementing the equivalent circuit shown in Figure 4 for the monolithic two stage amplifier is shown in Figure 5. The monolithic design made use of via-holes for source grounding, air-bridges for interconnect and MIM capacitors for RF grounding and dc blocking. The two stage amplifier layout has redundancy of transmission lines and air-bridges put in place to facilitate tuning on the MMIC if required. Eventually no tuning was required to meet the expected goals from the two stage MMIC. This success is attributed to the accurate device modeling and the consistency of the sub .2um MESFETs. The chip size for this monolithic chip is 1 x 0.5 mm which equates to 14dB of gain per square millimeter.

The gain and return loss of the amplifier is shown in Figure 6. The gain and noise figure of the amplifier is shown in Figure 7. This monolithic chip has demonstrated gain better than 7 dB with a worst case noise figure of 7.5 dB across the 40 to 60 GHz band. These results are consistent with the hybrid noise data. The higher noise measurement is due to the second stage contribution. A power compression curve for the amplifier at 60 GHz is shown in Figure 8. The one-dB compression point is +8 dBm and the saturated power is +10 dBm at 60 GHz. This represents the worst case power conditions, since the power at the lower end of the operating bandwidth is higher.

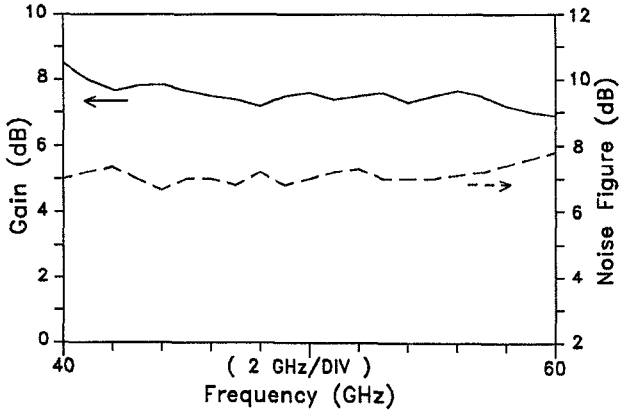


Figure 7. Measured gain and noise performance for the monolithic two stage amplifier using 75 um MESFET devices.

CONCLUSIONS

A monolithic broadband LNA using MESFET technology has been demonstrated at U-band. This monolithic chip has demonstrated better than 7 dB gain with less than 1.5dB ripple and a worst case noise figure of 7.5dB across the 40 to 60 GHz band. This chip has also demonstrated better than +8 dBm of output power across the U-band. Lower noise figure numbers are expected when such MMICs are processed using optimized low noise MESFET devices. These are state of the art results for MESFETs and millimeter-wave amplifier technologies.

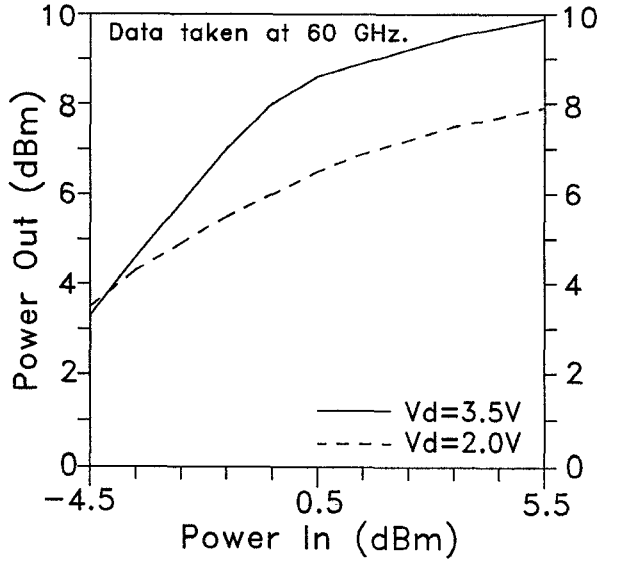


Figure 8. Compression data for the monolithic amplifier operating from 40 to 60 GHz.

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